Customer No.: 31561
Docket No.:13154-US-PA
Application No.: 10/710,931

AMENDMENTS

In The Claims

1. (currently amended) A metal-oxide-semiconductor (MOS) device for an electrostatic discharge (ESD) protection circuit with the MOS device serving as a clamping device in the ESD protection circuit, comprising:

a first conductive type substrate;

a gate structure, disposed over the substrate;

a second conductive type source region and a second conductive type [[~~source~~]]drain region, separately disposed in the substrate on each side of the gate structure;

a second conductive type doped layer, disposed in the substrate underneath the source region and the drain region but apart from the source region and the drain region; and

a second conductive type extended doped region, disposed in the substrate adjacent to the doped layer and the source region;

wherein, under a circuit connection, the drain region, the substrate and the source region together form a first parasitic bipolar junction transistor (BJT) and the drain region, the substrate and the doped layer together form a second parasitic bipolar junction transistor so that a current flowing into the drain region is channeled to a common voltage terminal via the first parasitic BJT and the second parasitic BJT.

2. (original) The MOS device of claim 1, wherein the substrate, the gate structure, the source region and the extended doped region are coupled to the common voltage terminal.

3. (original) The MOS device of claim 1, wherein the first conductive type is a p-doped

material and the second conductive type is an n-doped material.

4. (original) The MOS device of claim 1, wherein the first conductive type is an n-doped material and the second conductive type is a p-doped material.

5. (original) The MOS device of claim 1, wherein the gate structure comprises a bottom gate dielectric layer and a top gate conductive layer.

6. (original) A metal-oxide-semiconductor (MOS) device for an electrostatic discharge (ESD) protection circuit with the MOS device serving as a clamping device, comprising:

a first conductive type substrate;

a plurality of parallel-connected transistors, disposed on the substrate with each transistor having:

a gate structure disposed over the substrate;

a second conductive type source region and a second conductive type drain region, separately disposed in the substrate on each side of the gate structure;

a second conductive type doped layer, disposed in the substrate underneath the transistors but apart from the source regions and the drain regions; and

a second conductive type extended doped region, disposed in the substrate adjacent to the doped layer and the source region of the outmost transistors among the parallel-connected transistors;

wherein, under a circuit connection, the drain region, the substrate and the source region of the various transistors form at least a first parasitic bipolar junction transistor and at least one

the drain region of the various transistors, the substrate and the doped layer ~~of various transistor at least~~ form at least a second parasitic bipolar junction transistor so that currents flowing into various drain regions of the transistors are channeled to a common voltage terminal via the first parasitic bipolar junction transistor and the second parasitic bipolar junction transistor.

7. (original) The MOS device of claim 6, wherein the substrate and the gate structure, the source region, the extended doped region of the transistors are coupled to the common voltage terminal.

8. (original) The MOS device of claim 6, wherein the first conductive type is a p-doped material and the second conductive type is an n-doped material.

9. (original) The MOS device of claim 6, wherein the first conductive type is an n-doped material and the second conductive type is a p-doped material.

10. (original) The MOS device of claim 6, wherein the gate structure comprises a bottom gate dielectric layer and a top gate conductive layer.

11. (original) The MOS device of claim 6, wherein every adjacent pair of transistors either uses a common source region or a common drain region.

12. (new) The MOS device of claim 1, wherein the common voltage is a ground voltage.

13. (new) The MOS device of claim 6, wherein the common voltage is a ground voltage.